AMENDMENTS TO THE CLAIMS

1-33. (canceled)

34. (currently amended) A signaling circuit for encoding presence detect data comprising:

a first signal encoding portion for encoding first presence detect information, said first presence detect information being disposed in a ~~hard-wired~~ hardwired circuit of an integrated circuit semiconductor memory device during the manufacturing of said integrated circuit semiconductor memory device, ~~said hard-wired circuit formed during manufacturing of said semiconductor memory device~~, said first present detect data having one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit; and

a second signal encoding portion for encoding second presence detect information, said second presence detect information being disposed in a programmable circuit of said semiconductor memory device, said programmable circuit programmed subsequent to manufacturing of said semiconductor memory device.

35. (currently amended): A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a storage capacity of said integrated circuit semiconductor memory device.

36. (currently amended) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data bus width of said integrated circuit semiconductor memory device.

37. (currently amended) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data access speed of said integrated circuit semiconductor memory device.

38. (currently amended) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a column address strobe latency of said integrated circuit semiconductor memory device.

39. (currently amended) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data refresh rate of said integrated circuit semiconductor memory device.

40. (currently amended) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to an interface voltage of said integrated circuit semiconductor memory device.

41. (previously presented) A signaling circuit as defined in claim 34 wherein said first signal encoding portion and said second signal encoding portion comprise first and second serial data signals respectively, said first and second serial data signals being adapted to be transmitted over a single data line.

42. (previously presented) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises a fuse device.

43. (previously presented) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises an antifuse device.

44. (previously presented) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises a transistor-based device.

45-52 (canceled)

53. (currently amended) A method of operating a memory integrated circuit comprising:

receiving a first signal at a memory controller from said memory integrated circuit, said first signal encoding first presence detect information hardwired into said memory integrated circuit during manufacturing of said memory integrated circuit, wherein said first present detect data has one of a first value associated with a short circuit within said memory integrated circuit and a second value associated with an open circuit within said memory integrated circuit; and

receiving a second signal at a memory controller from said memory integrated circuit, said second signal encoding second presence detect information programmed into said memory integrated circuit subsequent to manufacturing of said memory integrated circuit.

54. (previously presented) A method of operating a memory integrated circuit as defined in claim 53 further comprising:

receiving a control signal at said memory integrated circuit from said memory controller, said control signal being related to at least one of said first signal and said second signal.

55. (previously presented) A method of operating a memory integrated circuit as defined in claim 53 further comprising:

receiving an address signal at said memory integrated circuit from said memory controller, said address signal having a format related to at least one of said first signal and said second signal.

56. (previously presented) A method of operating a memory integrated circuit as defined in claim 53 further comprising:

recognizing an identity of said memory integrated circuit at said memory controller based on said first and second signals.

57- 59 (canceled)